IN THE CLAIMS:

Please cancel claims 1-3 without prejudice.

Please add the following new claims 4-53.

--4. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and

a reference array operatively coupled to the memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells.

5. The system of claim 4, wherein the reference array comprises a plurality of reference cells, and wherein the reference cells and memory cells selected for programming are biased with approximately similar bias conditions on their control gates, common lines, and bit lines.

6. The system of claim 5, wherein the each set of reference cell and associated memory cell shares the same common line and control gate line.

7. The system of claim 4, further comprising:

a first address decoder operatively coupled to the plurality of bit lines, the first address decoder configured to receive an input address and select one or more bit lines.

8. The system of claim 4, further comprising:

a second address decoder operatively coupled to the at least one common line, the second address decoder configured to receive an input address and select one or more common lines.

9. The system of claim 4, further comprising:

a third address decoder operatively coupled to the plurality of control gate lines, the third address decoder configured to receive an input address and select one or more control gate lines.

10. The system of claim 4, further comprising:

a reference generator coupled to the at least one memory decoder and the reference array, the reference generator configured to provide a first set of signals to the reference array and the bias signals to the at least one memory decoder.

11. The system of claim 10, furthering comprising:

a voltage multiplier configured to receive an input voltage and generate an output voltage, wherein the output voltage is higher than the input voltage and is used for a combination of erase, program, and read operations.

12. The system of claim 11, wherein the voltage multiplier is implemented using switched capacitor circuits.

13. The system of claim 11, furthering comprising:

a voltage control circuit coupled to voltage multiplier and reference generator, the voltage control circuit configured to provide a reference signal from the reference generator or a high voltage to the memory cells.

14. The system of claim 13, wherein the voltage control circuit is configured to provide the high voltage to a control gate for an erase operation.

15. The system of claim 13, wherein the voltage control circuit is configured to provide a high voltage pulse to a common line for a programming operation.

16. The system of claim 4, wherein each memory array includes a plurality of segments, each segment including P rows by Q columns of memory cells.

17. The system of claim 16, wherein the plurality of bit lines comprise

a set of main bit lines that traverses a length of each memory array, and

sets of segmented bit lines, each segmented bit line traversing a portion of the length of the memory array and coupled to one main bit line at one or more selected locations.

18. The system of claim 17, further comprising:

a plurality of bit line select transistors coupling the segmented bit lines to the main bit lines.

19. The system of claim 18, wherein the bit line select transistors are also used as cascoding transistors to isolate bit line capacitance.

20. The system of claim 16, wherein the at least one common line comprises

at least one main common line that traverses the width of the memory array, and

a plurality of segmented common lines for each main common line, each segmented common line traversing a portion of the width of the memory array and coupled to one main common line at one or more selected locations.

21. The system of claim 4, further comprising:

a plurality of current sinks disposed along each of the at least one common line.

22. The system of claim 16, further comprising:

a set of main control gate lines that traverses a width of the memory array, each main control gate line coupled to a set of memory cells located along a row of the memory array.

23. The system of claim 22, further comprising:

a set of segmented control gate lines for each control gate line, each segmented control gate line traversing a portion of the width of the memory array.

24. The system of claim 16, further comprising:

at least one inhibit line coupled to memory cells within the memory arrays.

25. The system of claim 24, wherein each inhibit line couples to memory cells in two or more segments.

26. The system of claim 24, wherein each inhibit line couples to memory cells within one memory array.

27. The system of claim 16, further comprising:

a plurality of inhibit enable lines, one inhibit enable line for each bit line.

28. The system of claim 4, wherein each common line is driven from both sides of a memory array.

29. The system of claim 4, wherein the reference array includes

a plurality of reference cells, each reference cell operative to provide one reference signal.

30. The system of claim 29, wherein the reference cells are disposed at approximately linearly spaced locations along the at least one common line.

31. The system of claim 29, wherein the reference cells are disposed at approximately geometrically spaced locations along the at least one common line.

32. The system of claim 29, further comprising:

a plurality of reference lines coupled to the plurality of reference cells, wherein resistance of the reference lines is approximately matched to resistance of common lines.

33. The system of claim 32, wherein each reference cell is disposed at a location in an associated reference line such that voltage drops at both ends of the reference line are approximately equal.

34. The system of claim 29, wherein each reference signal is generated by averaging outputs from two or more reference cells.

35. The system of claim 4, wherein the reference array includes:

a plurality of reference cells operative to provide the reference signals, wherein at least one of the reference signals is generated by extrapolating outputs from two reference cells.

36. The system of claim 4, wherein the reference signals define 2^N unique levels used for programming and reading the memory cells.

37. The system of claim 4, wherein the reference signals define 2^N-1 unique levels used for programming and reading the memory cells.

38. The system of claim 5, wherein the reference cells are programmed with a set of reference values.

39. The system of claim 38, wherein reference cells previously programmed are inhibited from further programming.

40. The system of claim 4, further comprising:

a plurality of drivers coupled to the plurality of bit lines, each driver configured to control an associated bit line during write, read, or erase operation.

41. The system of claim 40, wherein each driver comprises:

a plurality of N data latches configured to receive and latch N data bits from a memory cell during a read operation.

42. The system of claim 40, wherein each driver further comprises:

a voltage comparator coupled to the associated bit line and a reference source, the voltage comparator configured to compare a voltage on the bit line and one of the reference signals from the reference array and to provide a comparison result.

43. The system of claim 42, wherein each driver further comprises:

a multiplexer operative to receive the reference signals from the reference array and to provide one of the reference signals to the voltage comparator.

44. The system of claim 40, wherein each driver is associated with one memory cell during programming, and wherein each driver further comprises:

an inhibit circuit operative to enable or inhibit programming of a particular memory cell coupled to the associated bit line.

45. The system of claim 40, wherein each driver is associated with one memory cell during programming, and wherein each driver further comprises:

control circuitry configured to generate a first status signal indicative of a particular memory cell coupled to the associated bit line being placed in a program inhibit mode.

46. The system of claim 45, wherein the plurality of drivers are configured to generate a second status signal indicative of all memory cells associated with the plurality of drivers being placed in the program inhibit mode.

47. The system of claim 46, wherein the second status signal is generated by wired-ORing first status signals from the plurality of drivers.

48. The system of claim 46, wherein the first status signals from the plurality of drivers are each provided to a gate of a respective one of a plurality of pull-down transistors, and wherein the second status signal is generated by coupling drains of the pulldown transistors.